

COVER SHEET	1
BLOCK DIAGRAM	2
CLOCK MAP	3
POWER MAP	4
GPIO MAP	5
Intel Diamondville-CPU	6-7
VRM Single Phase	8
Intel Lakeport -GMCH	9-12
DDR II SO-DIMM	13-14
Mini PCIE Slot	15
LAN 8111C	16
VGA CONNECTOR	17
Clock Generator - ICS954120	18
ICH7R	19-21
TPM LPC Debug port	22
USB CONNECTORS	23
HD AUDIO CODEC(ALC 888)	24
+19V DC-IN	25
5DUAL-PCIRST#	26
F_ PANEL	27
SATA & CF_Card & FAN CONTROL	28
ACPI Controller	29
Auto BOM manual	30
PWOK MAP	31
History	32

MS-7418 (MS-6496)

Version 0B

CPU:

Intel Dimondville

System Chipset:

Intel 945GC (North Bridge)

Intel ICH7(South Bridge)

On Board Chipset:

BIOS -- SPI

HD AUDIO CODEC(ALC888)

LAN -- Realtek RTL8111C

Clock Generator - ICS954119

Main Memory:

DDR II SO-DIMM x 1 (Max 2GB)


CF Card Connector for flash Memory

Expansion Slots:

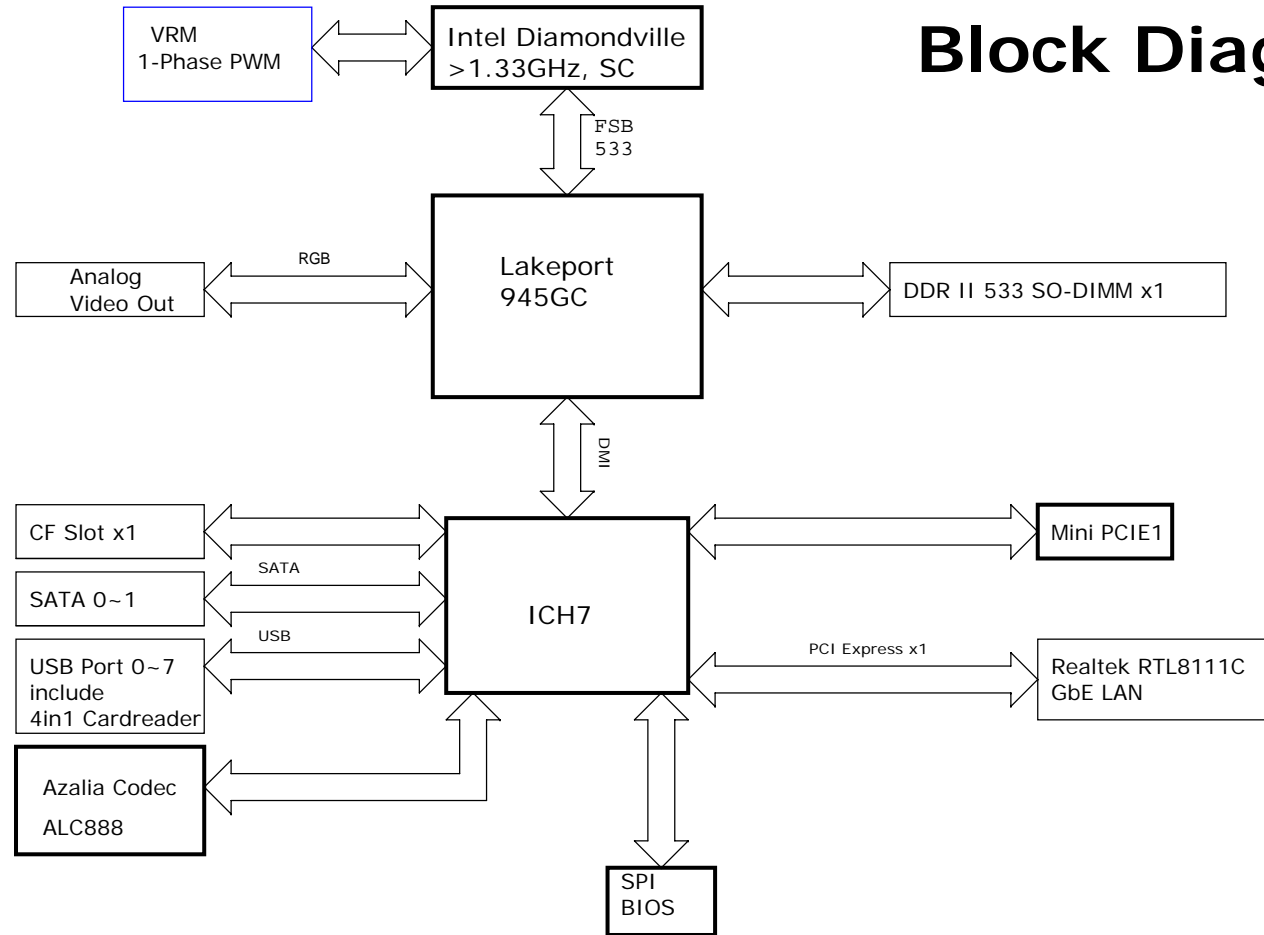
Internal Mini PCIE x1

Intersil PWM:

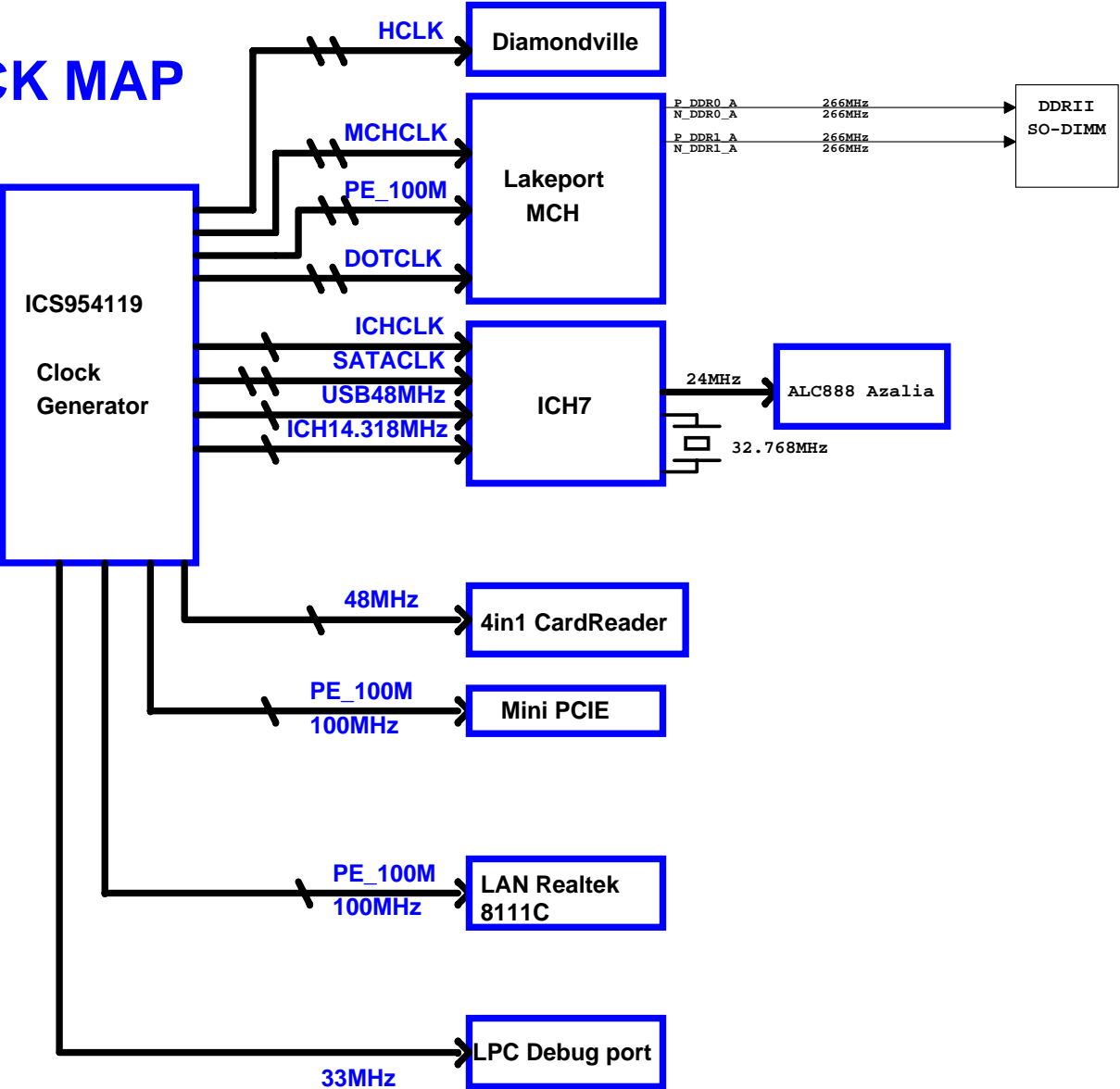
Controller: 6314

		MICRO-STAR INT'L CO., LTD.	
Title COVER SHEET			
Size	Document Number MS-7418		Rev 0B
Date:	Friday, April 11, 2008	Sheet	1 of 32

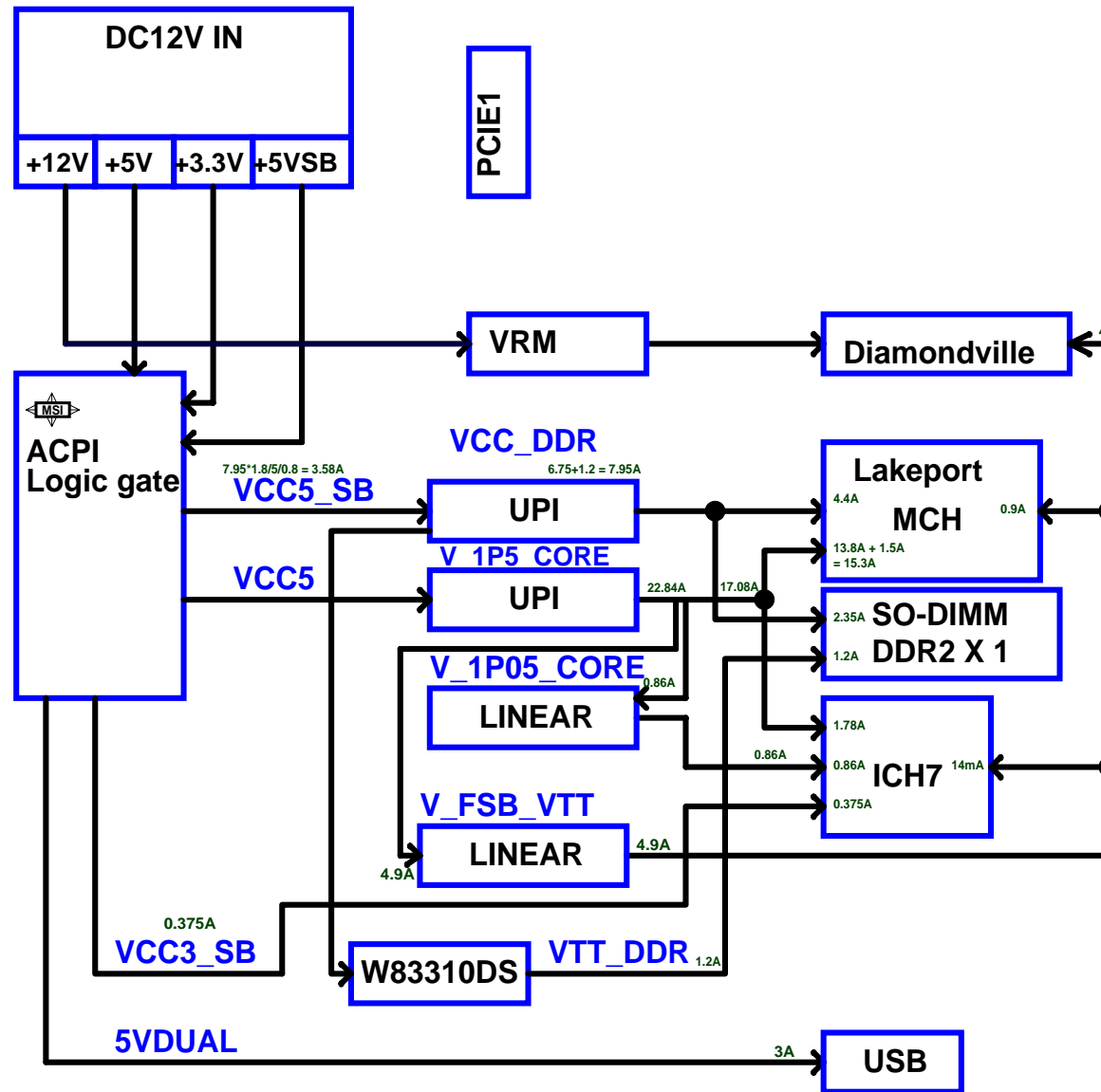
Block Diagram



CLOCK MAP



POWER MAP



ICH7

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Signal Name or status
GPIO[0]	SIO_SMI#	AB18	I/O	Vcc3p3	N	Y	5	Input	pull high VCC3
GPIO[1]	PCIREQ[5]#	C8	I/O	V5REF	N	Y	5	Input	PREQ#5
GPIO[2]	PIRQE#	G8	I/OD	V5REF	N	Y	5	Input	PIRQ#E
GPIO[3]	PIRQF#	F7	I/OD	V5REF	N	Y	5	Input	PIRQ#F
GPIO[4]	PIRQG#	F8	I/OD	V5REF	N	Y	5	Input	PIRQ#G
GPIO[5]	PIRQH#	G7	I/OD	V5REF	N	Y	5	Input	PIRQ#H
GPIO[6]	ATADET0	AC21	I/O	Vcc3p3	N	Y	3.3	Input	ATADET0
GPIO[7]	GPI7	AC18	I/O	Vcc3p3	N	Y	3.3	Input	pull high VCC3
GPIO[8]	SIO_PME#	E21	I/O	VccSus3p3	N	Y	3.3	Input	SIO_PME# pull high VCC3_SB
GPIO[9]	WLAN_PWRON	E20	I/O	VccSus3p3	N	Y	3.3	Output	pull high VCC3_SB
GPIO[10]	unmuxed	A20	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[11]	SMBALERT#	B23	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[12]	unmuxed	F19	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[13]	unmuxed	E19	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[14]	ADT7467_ALERT	R4	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[15]	unmuxed	E22	I/O	VccSus3p3	N	Y	3.3	Input	pull high VCC3_SB
GPIO[16]	unmuxed	AC22	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[17]	PCIGNT[5]#	D8	I/O	Vcc3p3	N	N	3.3	N/A	NC
GPIO[18]	unmuxed	AC20	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[19]	SATA1GP	AH18	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[20]	unmuxed	AF21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[21]	SATA0GP	AF19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[22]	PCIREQ[4]#	A13	I/O	Vcc3p3	N	N	3.3	Input	PREQ#4
GPIO[23]	LDRQ1#	AA5	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[24]	unmuxed	R3	I/O	VccSus3p3	N	N	3.3	No Change	NC
GPIO[25]	S1_3_LED	D20	I/O	VccSus3p3	Y	N	3.3	1	pull high VCC3_SB
GPIO[26]	unmuxed	A21	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[27]	unmuxed	B21	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[28]	unmuxed	E23	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[29]	OC#2	C3	I/O	VccSus3p3	N	N	3.3	Input	OC#5
GPIO[30]	OC#2	A2	I/O	VccSus3p3	N	N	3.3	Input	OC#6
GPIO[31]	OC#2	B3	I/O	VccSus3p3	N	N	3.3	Input	OC#7
GPIO[32]	CLEAR_CMOS#	AG18	I/O	Vcc3p3	N	N	3.3	1	CLEAR_CMOS#, ONLY pull high VCC3
GPIO[33]	unmuxed	AC19	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[34]	unmuxed	U2	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[35]	unmuxed	AD21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[36]	SATA2GP	AH19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[37]	SATA3GP	AE19	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[38]	unmuxed	AD20	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[39]	unmuxed	AE20	I/O	Vcc3p3	N	N	3.3	Input	pull high VCC3
GPIO[48]	GNT4#	A14	I/O	Vcc3p3	N	N	3.3	N/A	GNT4#
GPIO[49]	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	CPU	N/A	H_PWRGD
GPI[15..0] can configured to cause a SMI# or SCI.									

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39;36;23;21;19;7;0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31;29;15;8]: default as inputs and should be pulled up to VccSus3_3 if unused.

FWH Note: FWH GPs should only be used for static options, do not put dynamic nets on these				
GPIO	Pin#	Power	Tol	Signal Name
FPGI[0]	6	Main	3.3	pull-down
FPGI[1]	5	Main	3.3	pull-down
FPGI[2]	4	Main	3.3	pull-down
FPGI[3]	3	Main	3.3	pull-down
FPGI[4]	30	Main	3.3	pull-down

SIGNAL	DEVICE
MiniPCleRST#	MINI PCIE SLOT
TPMRST#	TPM
LANRST#	LAN 8111C
PCIRST_ICH7#	BUFFER IC
CF_RST#	CF_CARD
H_CPURST#	CPU
FWHRST#	LPT Debug port
MCHRST#	MCH

SMBCLK, SMBDATA, DDR2, PCIEX1, CLKGEN, ICH7, ADT7464

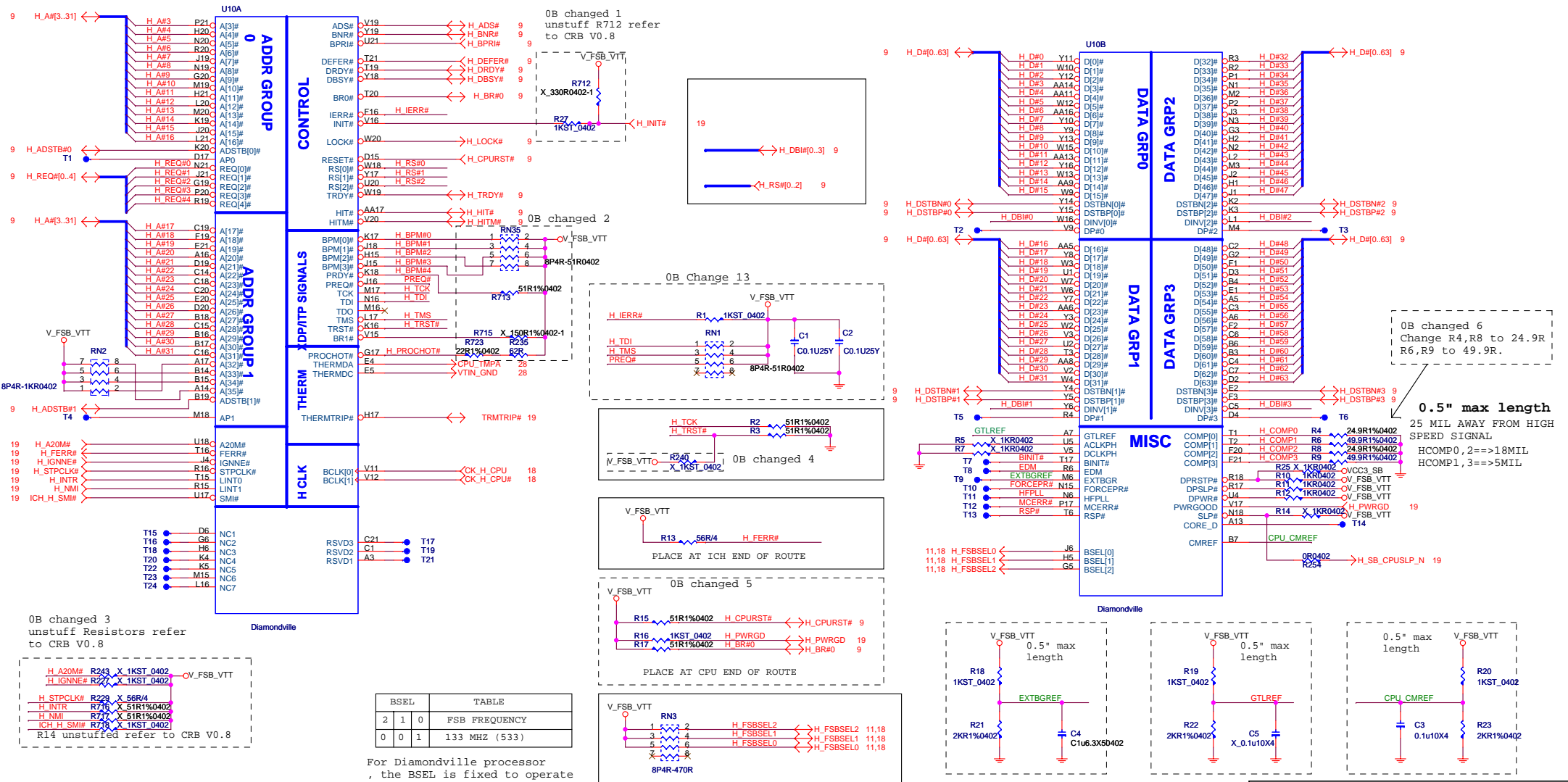
DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR
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CPU SIGNAL BLOCK



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Title	Intel LGA775 - Signals
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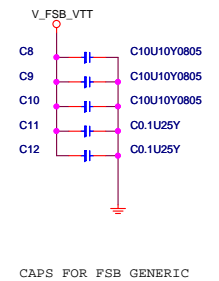
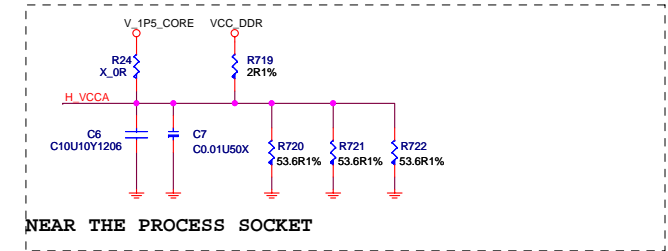
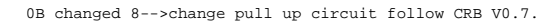
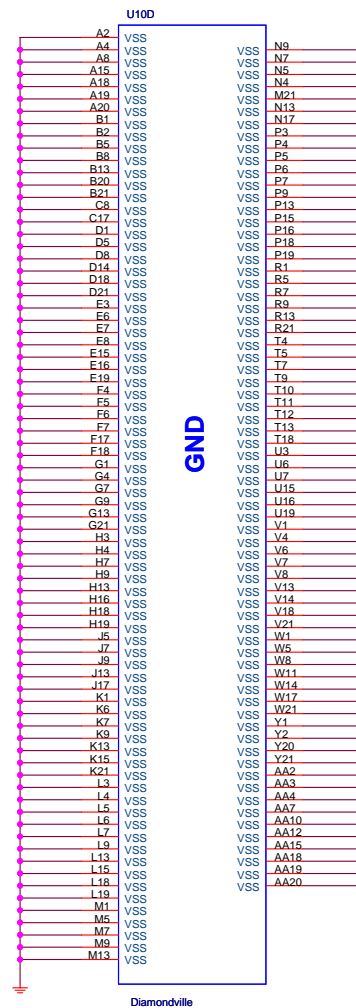
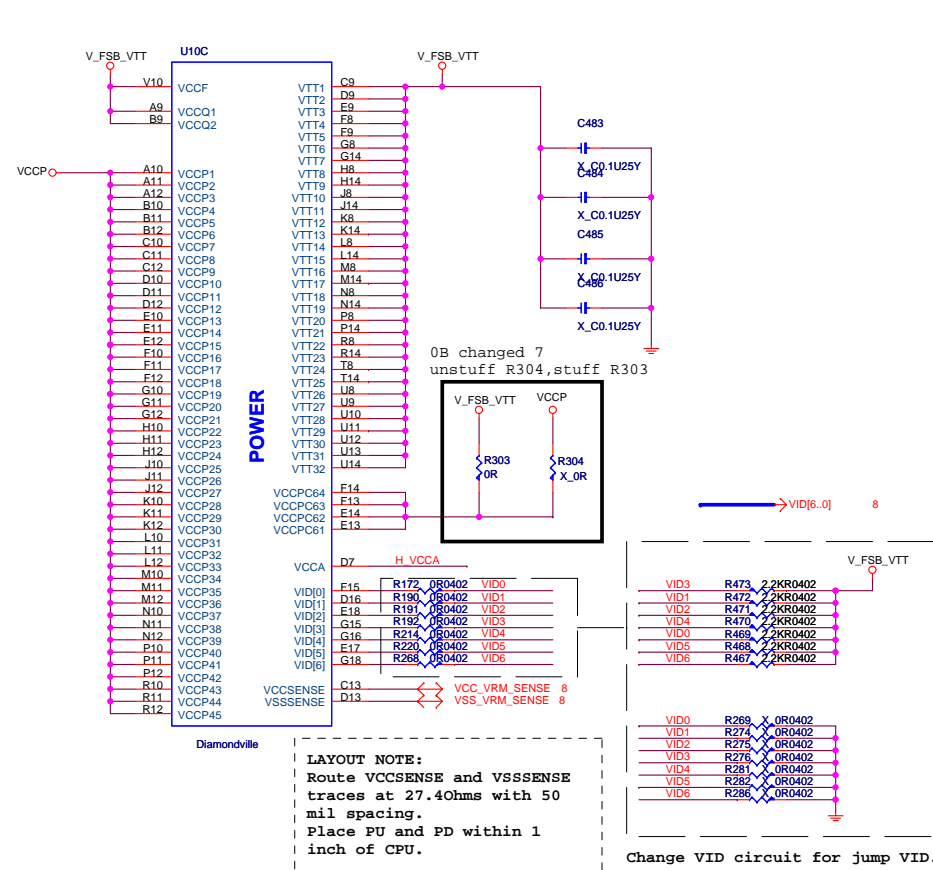
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MS-7418

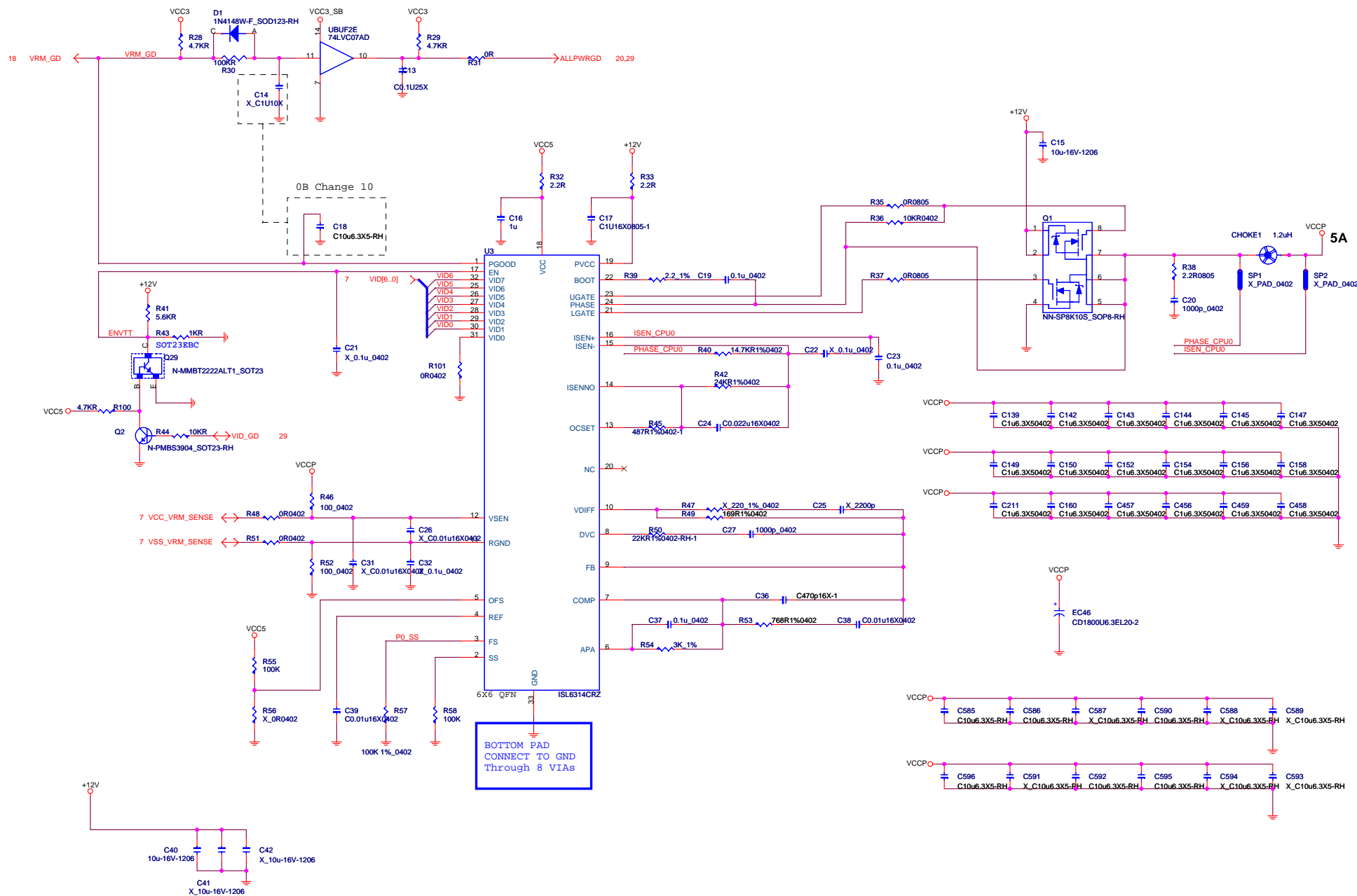
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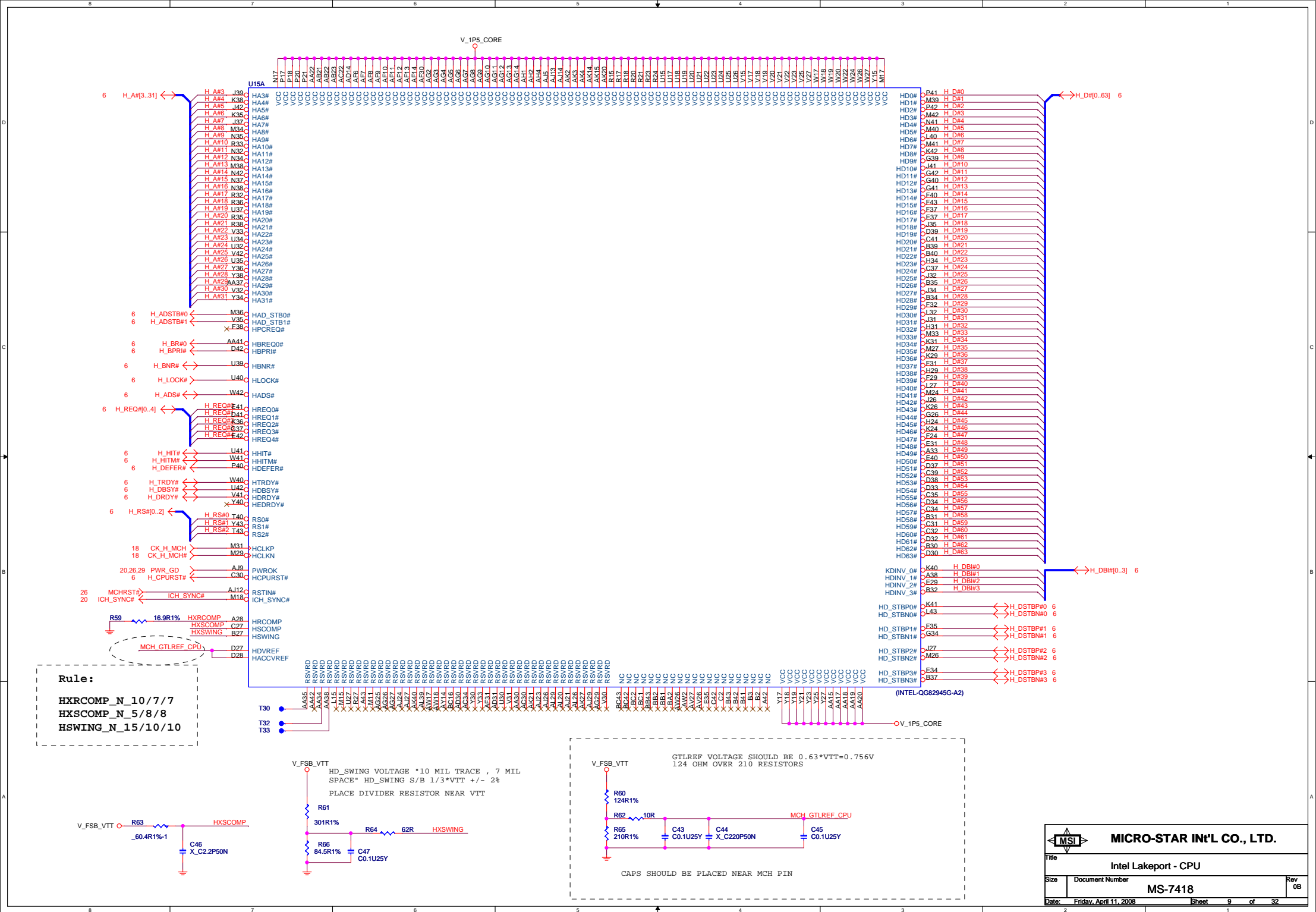
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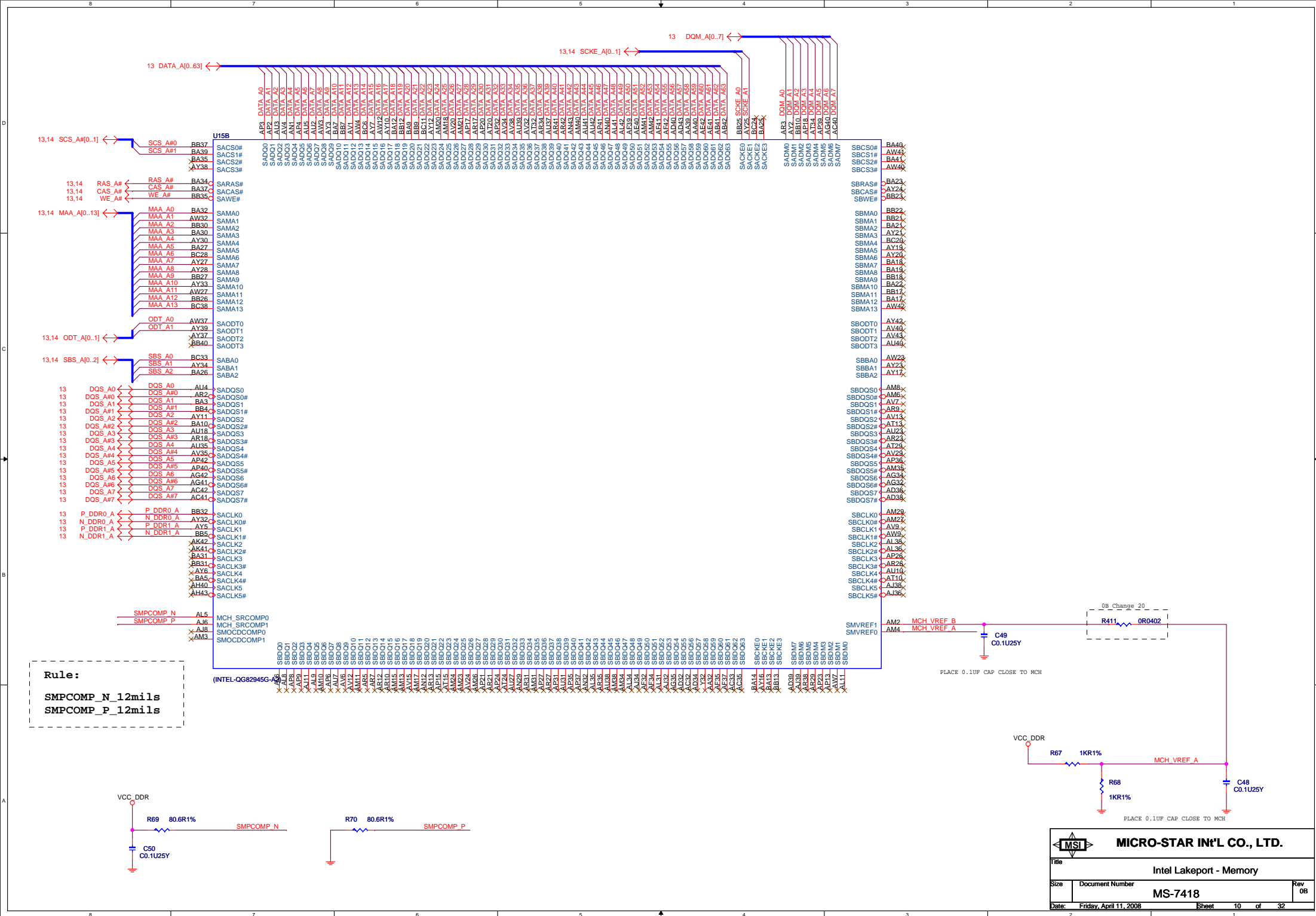
1



2.5A: before VCC stable
1.5A: after VCC stable

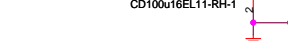
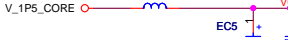
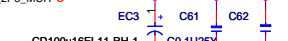
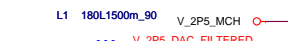
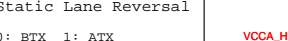
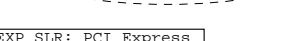
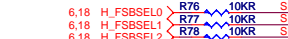


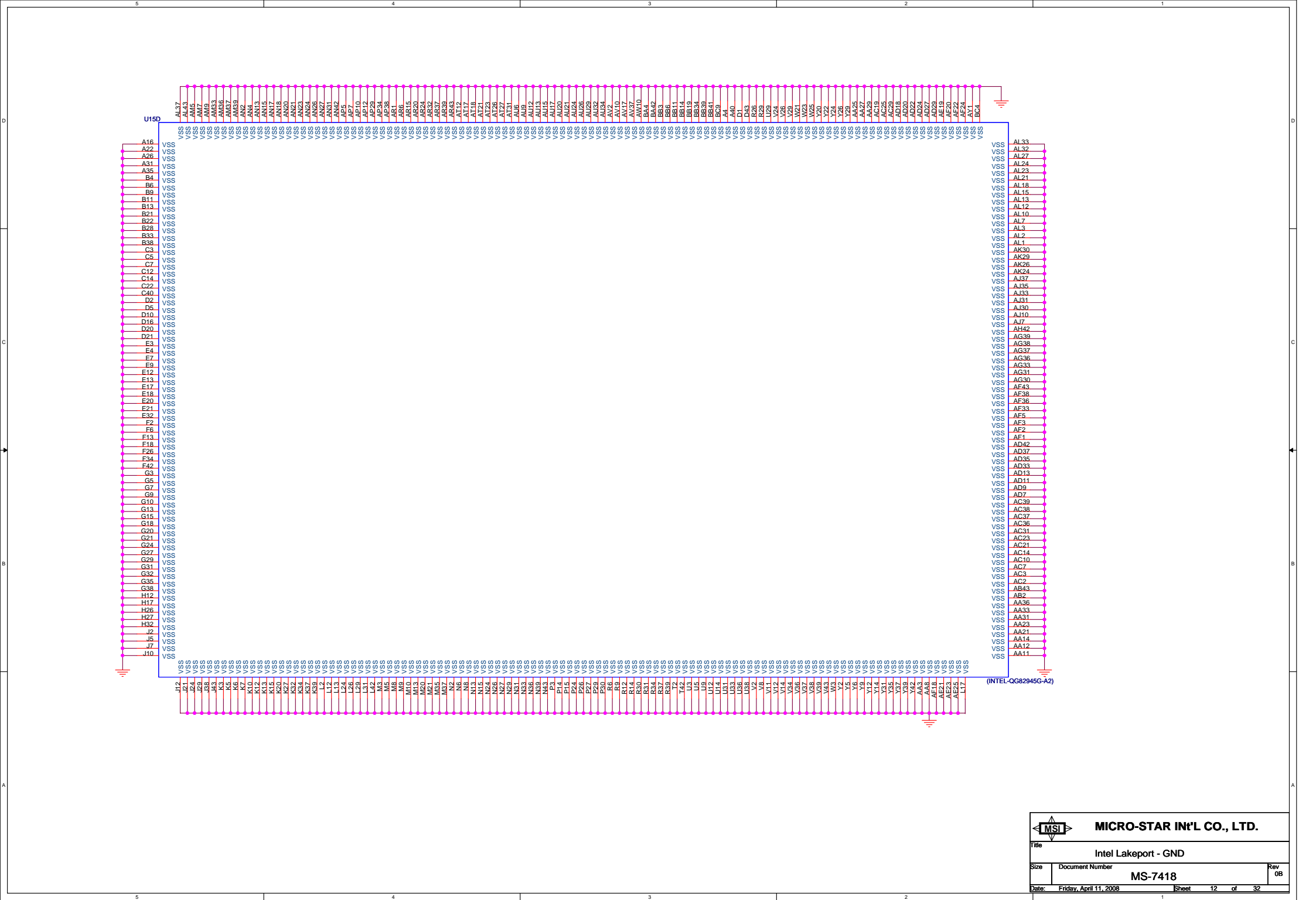




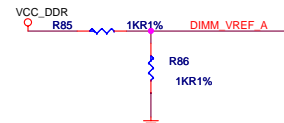
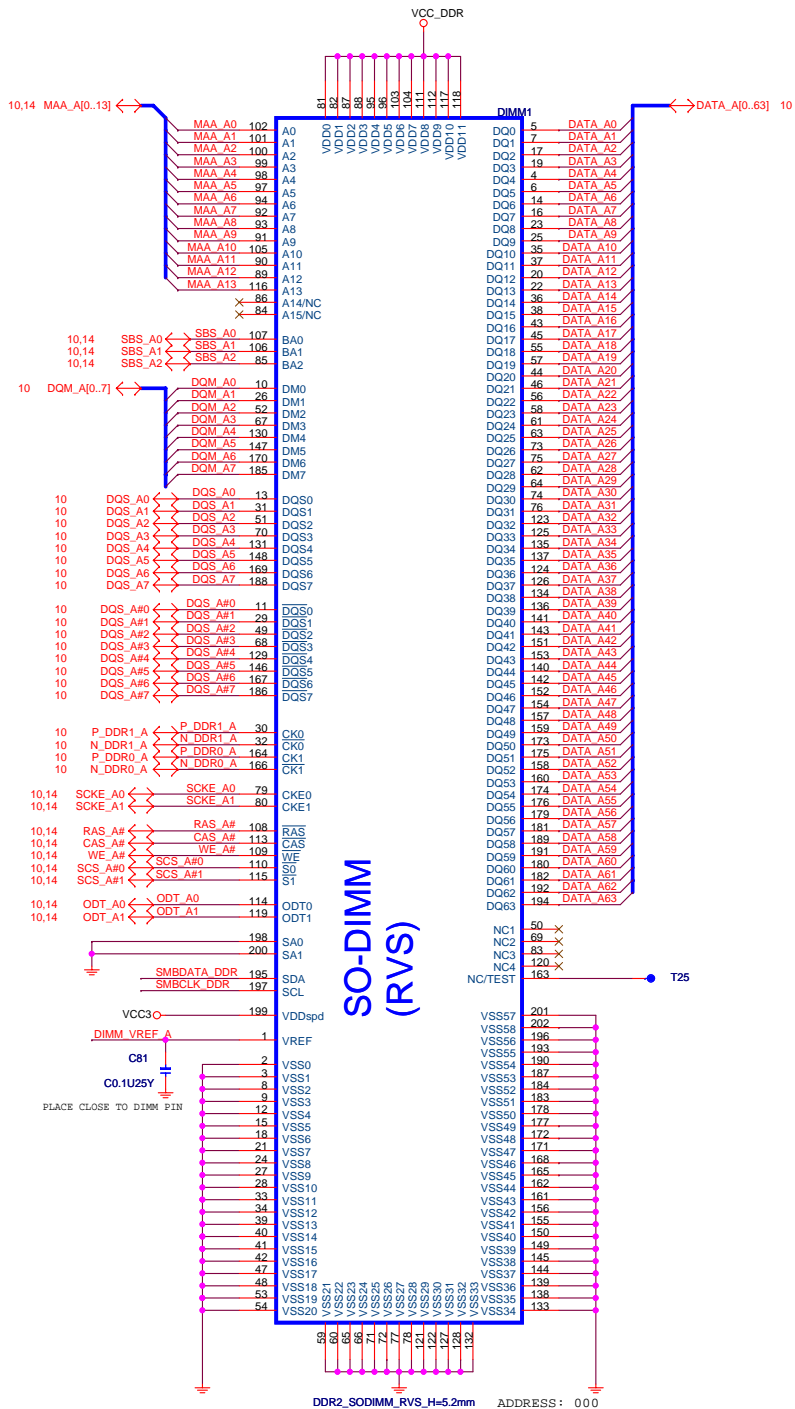
EXP_EN: PCI Express* SDVO
Concurrent Select

0: Only SDVO or PCI-E Operational
1: SDVO and PCI-E operating
simultaneously via PCI Express-G
port





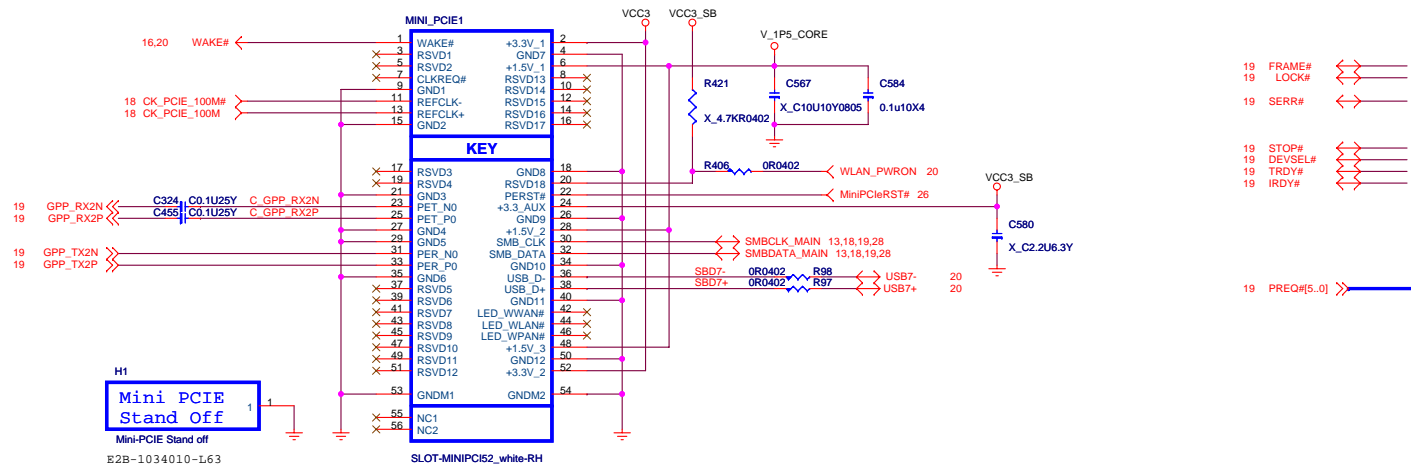
DDR2 SO-DIMM



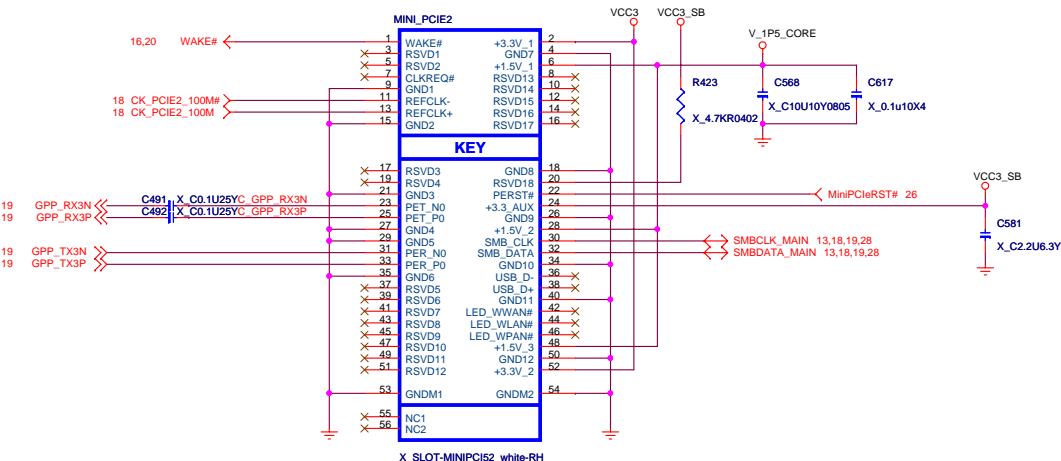
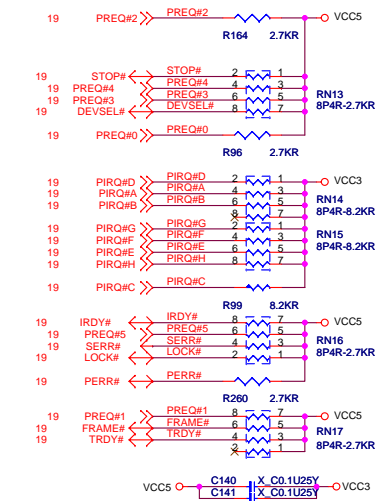
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DDR II SO-DIMM

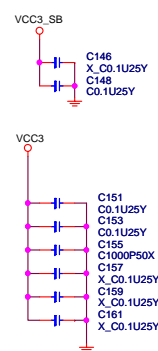
MS-7418

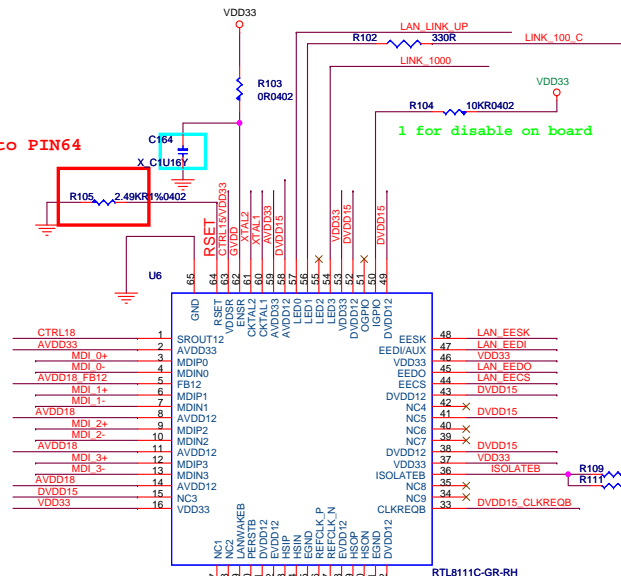


PCI PULL-UP / DOWN RESISTORS



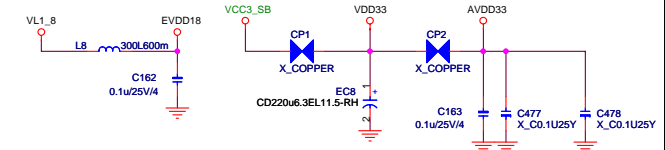
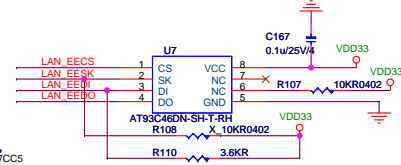
DECOUPLING CAPACITORS



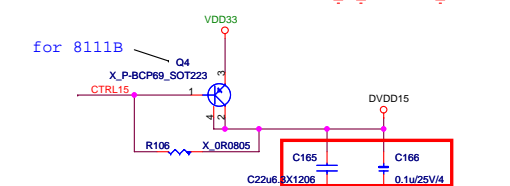
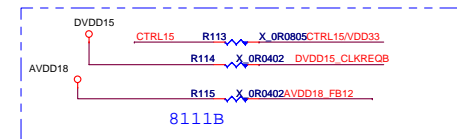


	RTL8111B / RTL8101E	RTL8111C	
AVDD33	3.3V	3.3V	
AVDD18	1.8V	1.2V	
EVDD18	1.8V	1.2V	
DVDD15	1.5V	1.2V	

	Q9	Q10
RTL8111B	<i>Need</i>	<i>Need</i>
RTL8111C	<i>N/A</i>	<i>N/A</i>



close to choke3 within 0.5cm

[illegible]

close to PIN63 within 0.5cm







VDD33 FB12 R116 AVDD18 FB12

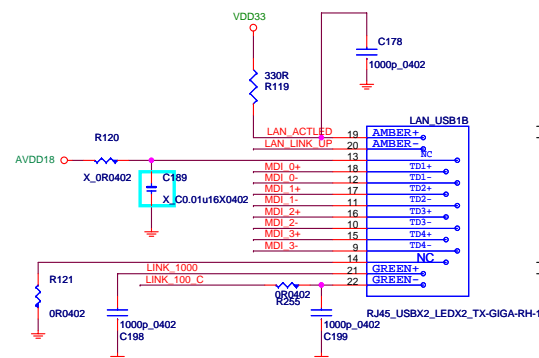
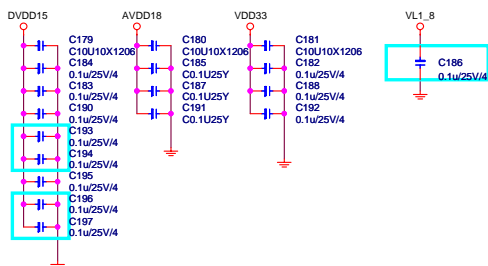
R117 0R0805 CTRL15/VDD33

AVDD18 DVDD15

R118 0R0805 C176 10µF C177 0.1µF

8111C C226 10µF

Power consumption			Giga-Lan		10/100-Lan	
	1G	100M	N58-22F0181-s42		N58-22F0061-s42 N58-22F0061-F02	
3.3V	103mA	TBD	Link	Yellow	Link	Yellow
1.5V	367mA	TBD	Active	Blinking	Active	Blinking
			1000	Orange	100	Green
1.8V	198mA	TBD	100	Green	10	None
			10	None		
			19		19	
			20	Yellow	20	Yellow
			21	Orange 	21	
			22	Green 	22	Green 



Video Connector

Power 20 mils

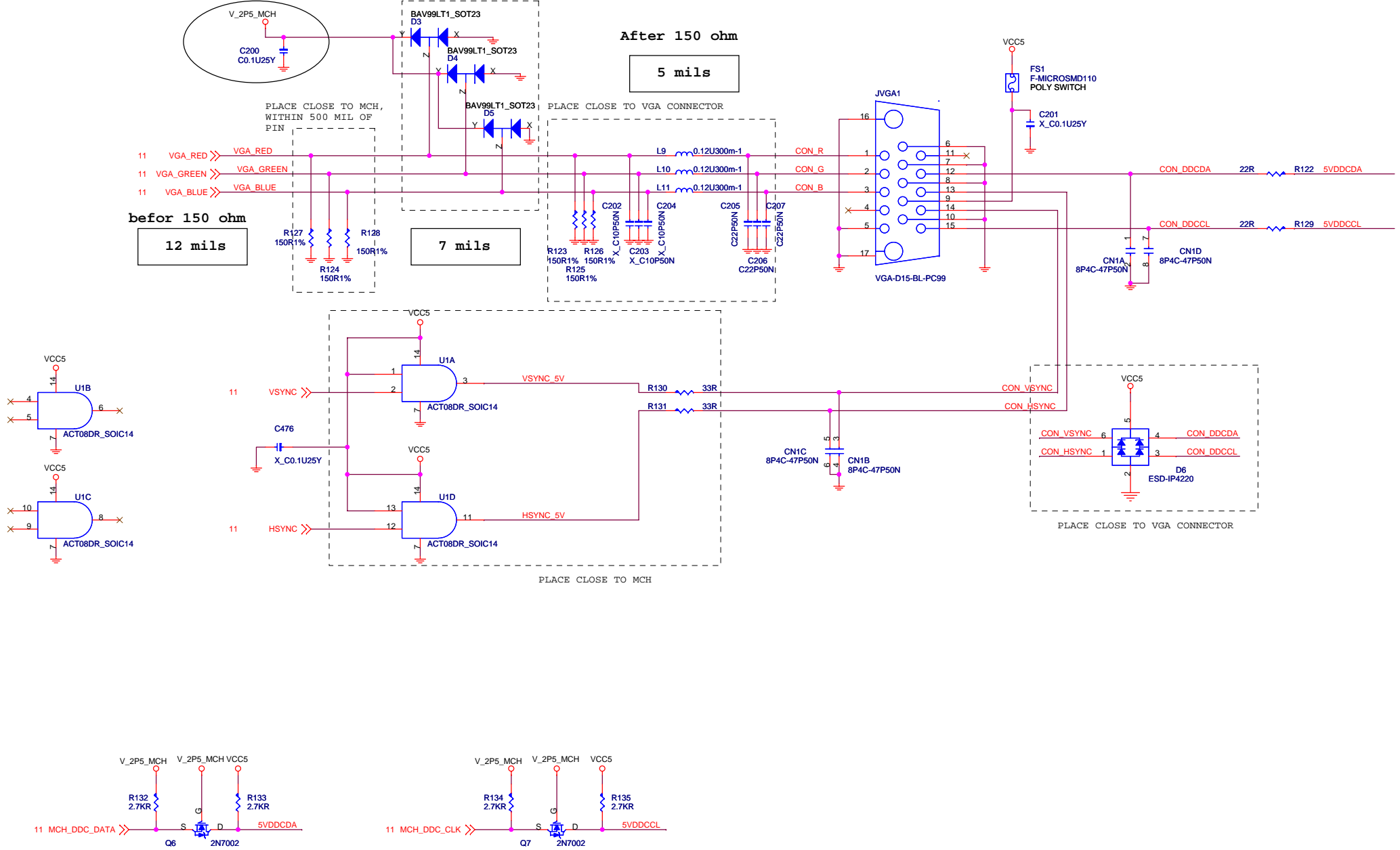
After 150 ohm

5 mils

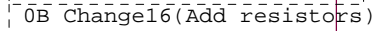
before 150 ohm

12 mils

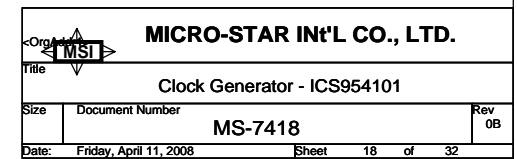
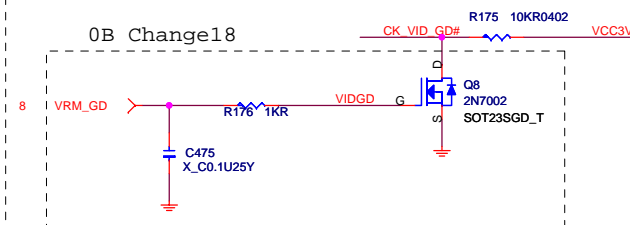
7 mils

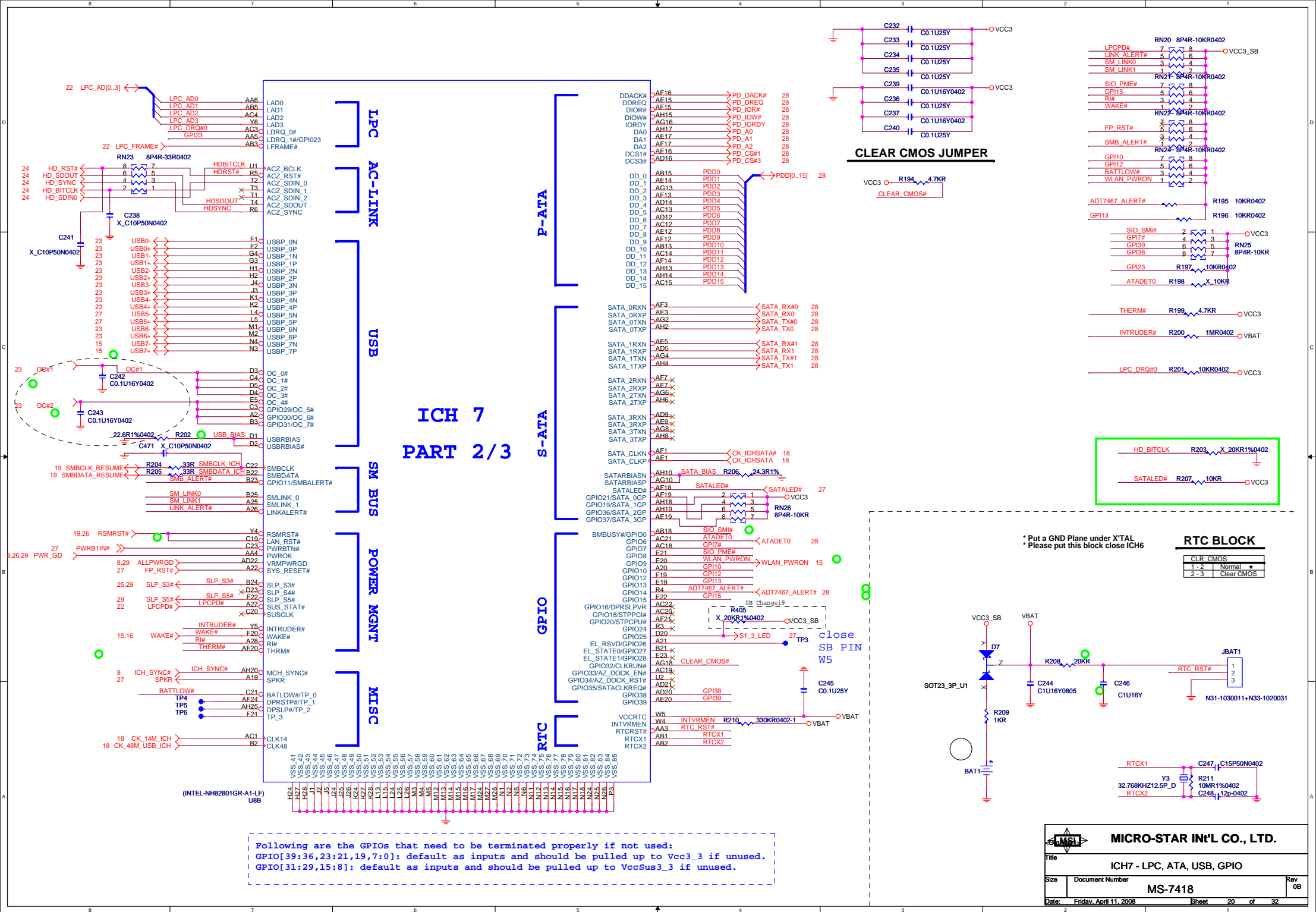


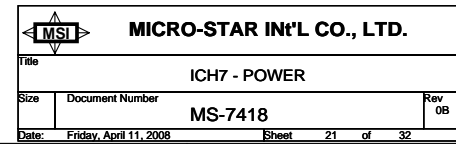
Trace length less than 0.5inches



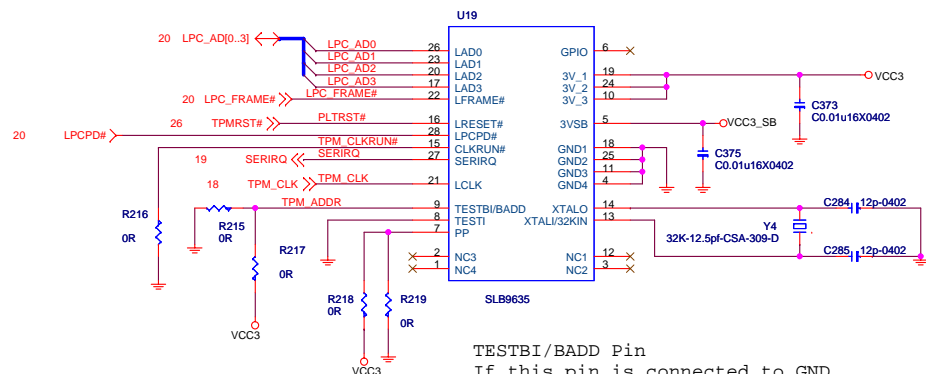
Pinout diagram for the 8P4R-1KR0402 connector. The diagram shows three rows of pins. The top row has pins 7 and 8, labeled RN18 and FSB. The middle row has pins 5 and 6, labeled FSA. The bottom row has pins 3 and 4, labeled FSC. The connector is labeled 8P4R-1KR0402 at the bottom.





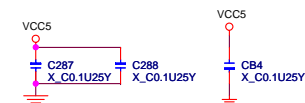
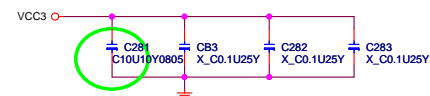
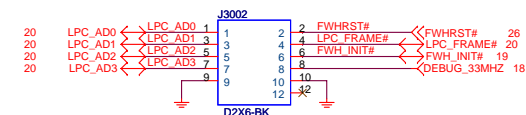


IO Address: 0x04E



TESTBI/BADD Pin
If this pin is connected to GND,
addresses 2EH/2FH are used.
If it is strapped to VCC,
addresses 4EH/4FH are used.

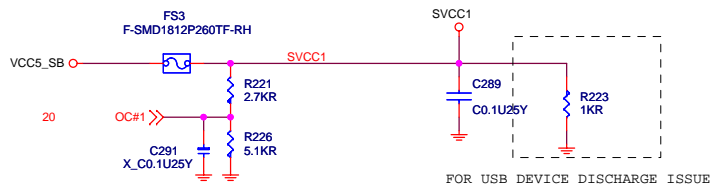
LPC Debug Port



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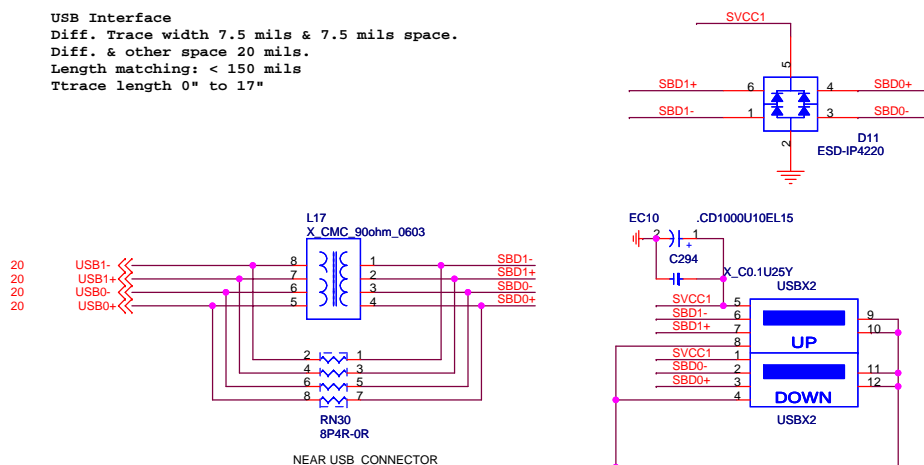
Title		FWH	
Size	Document Number	MS-7418	Rev 0B
Date:	Friday, April 11, 2008	Sheet 22 of 32	

POWER CIRCUIT FOR USB PORT 0,1,2,3 (REAR)



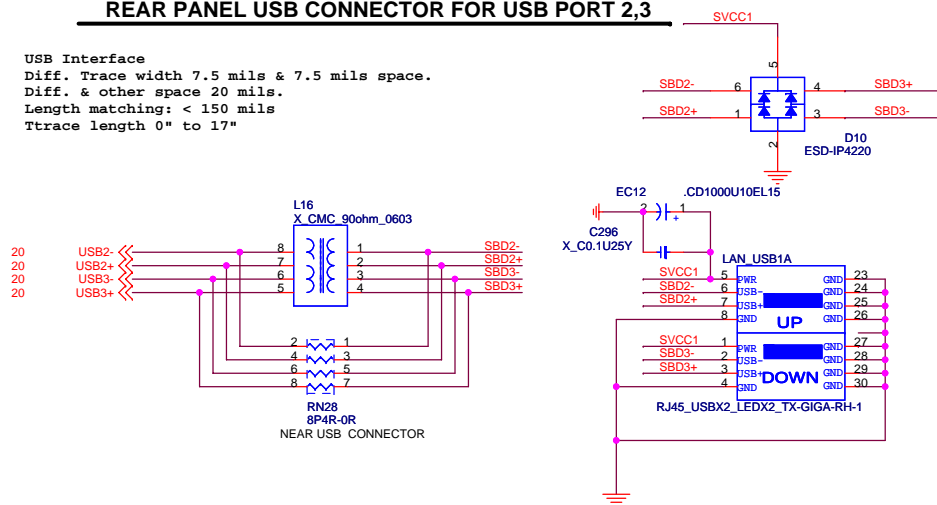
REAR PANEL USB CONNECTOR FOR USB PORT 0,1

USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Trace length 0" to 17"

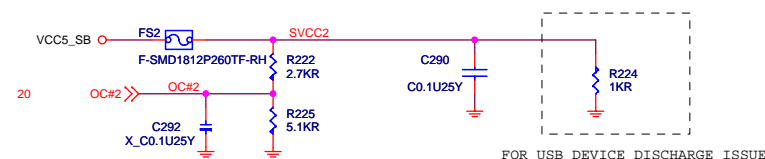


REAR PANEL USB CONNECTOR FOR USB PORT 2,3

USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Trace length 0" to 17"

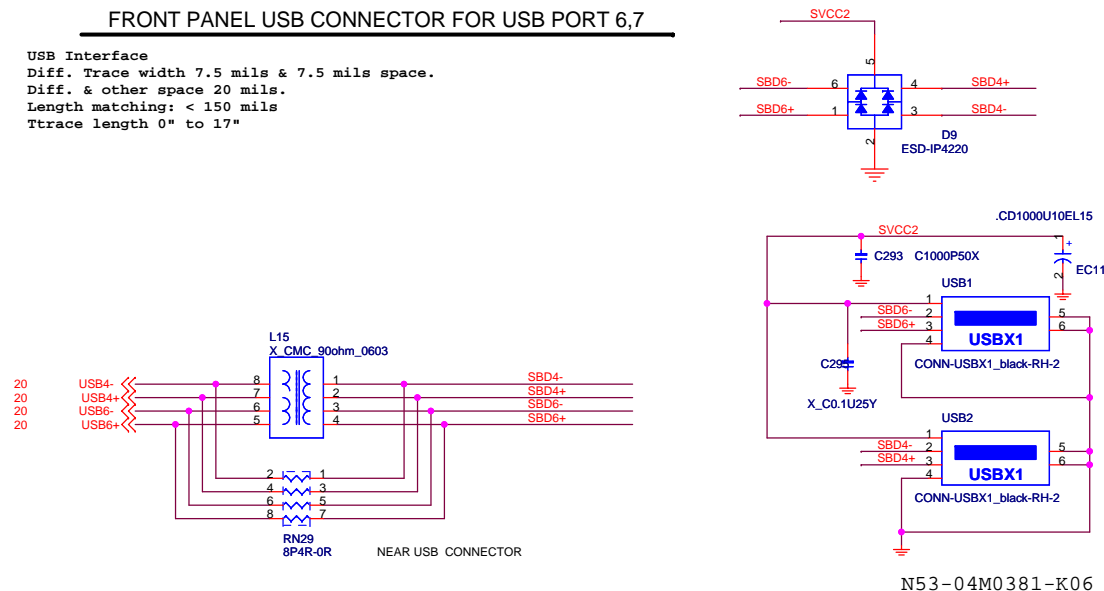


POWER CIRCUIT FOR USB PORT 4,6,7 (FRONT)



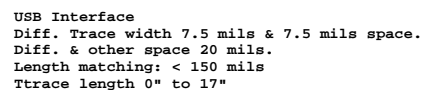
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Trace length 0" to 17"

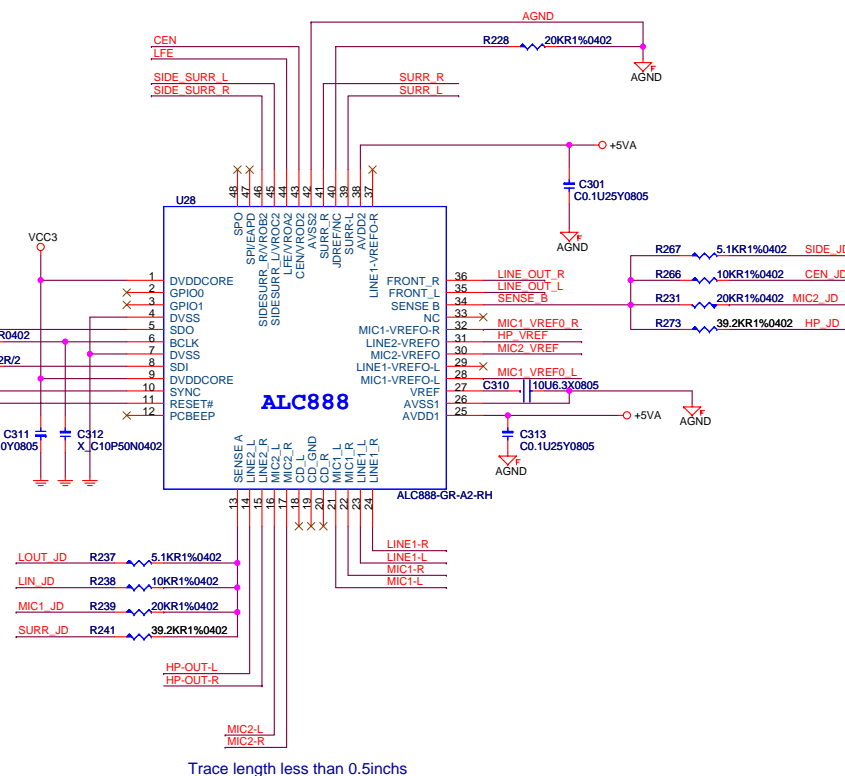


FRONT PANEL USB CONNECTOR FOR USB PORT 4

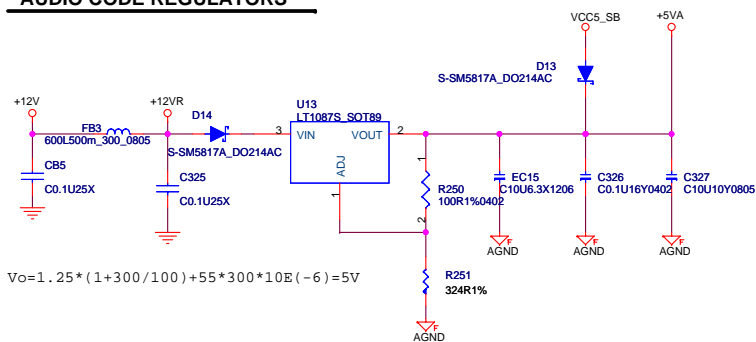
USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Trace length 0" to 17"



ALC888

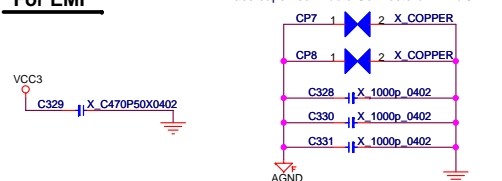


AUDIO CODE REGULATORS

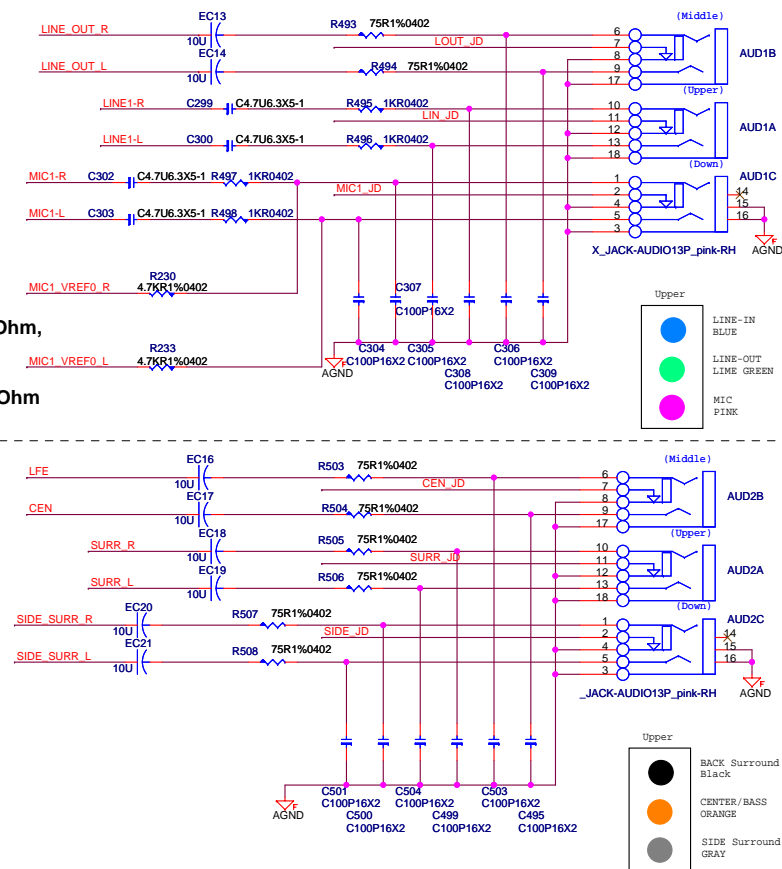


For EMI

Place caps near Audio Connector / MH4 / JMD1

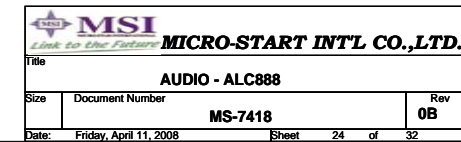
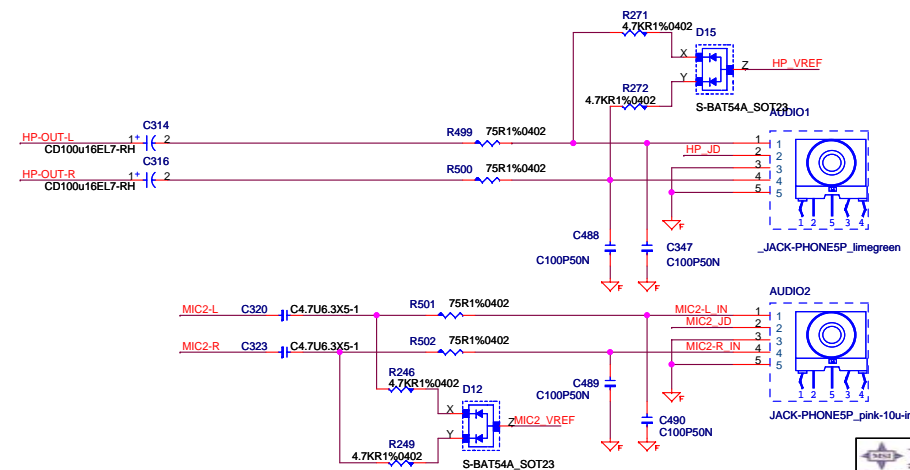


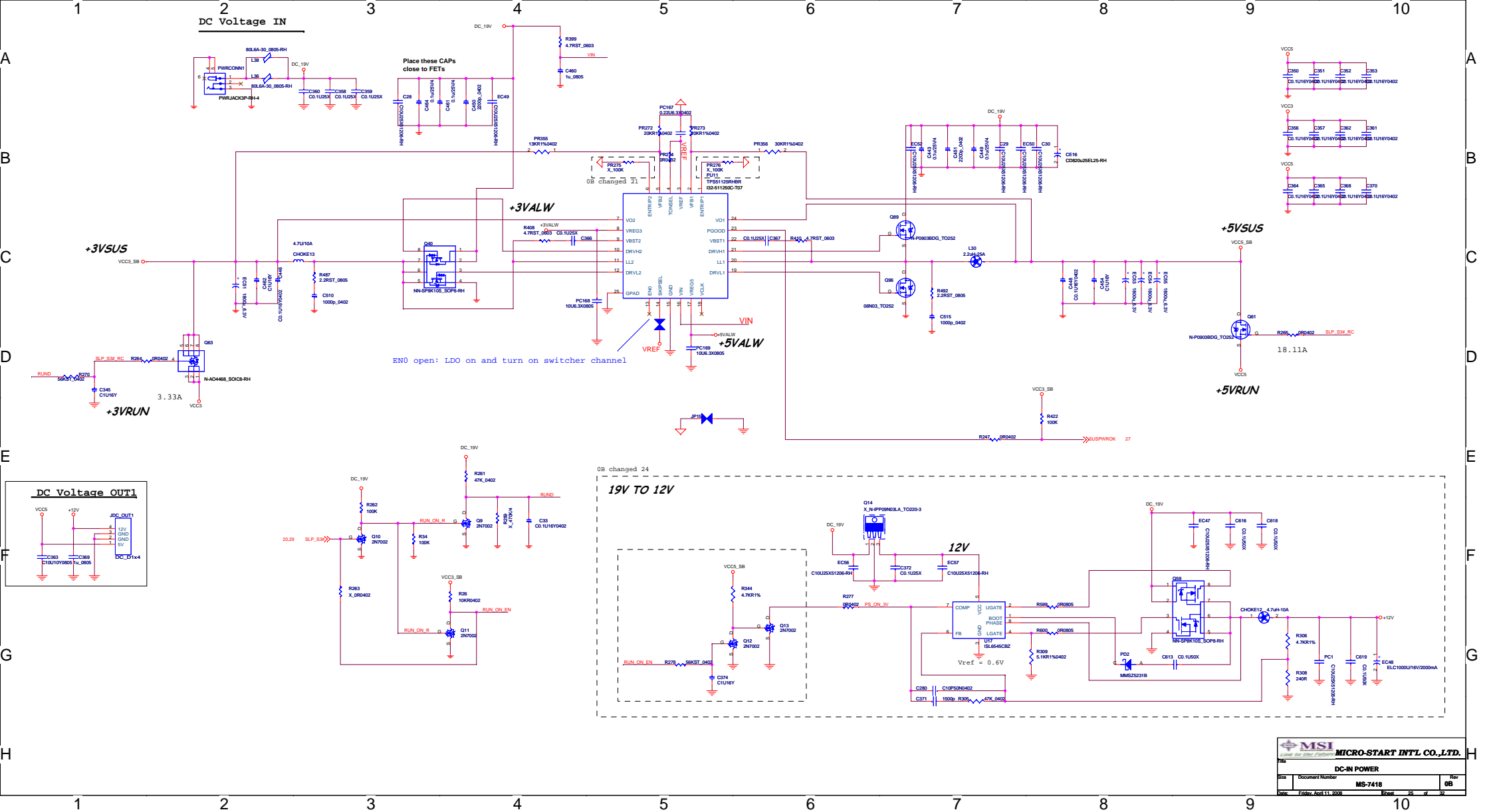
PHONE JACKER (HDA JACK)

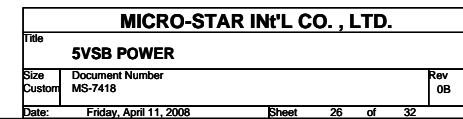
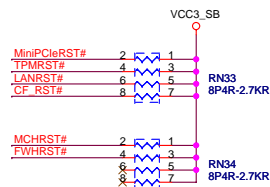


5.1 ch-->N54-13F0171-S42
R495&R496&R497&R498 =75 Ohm,

7.1 ch-->N54-26F0111-K06
R495&R496&R497&R498 =1K Ohm

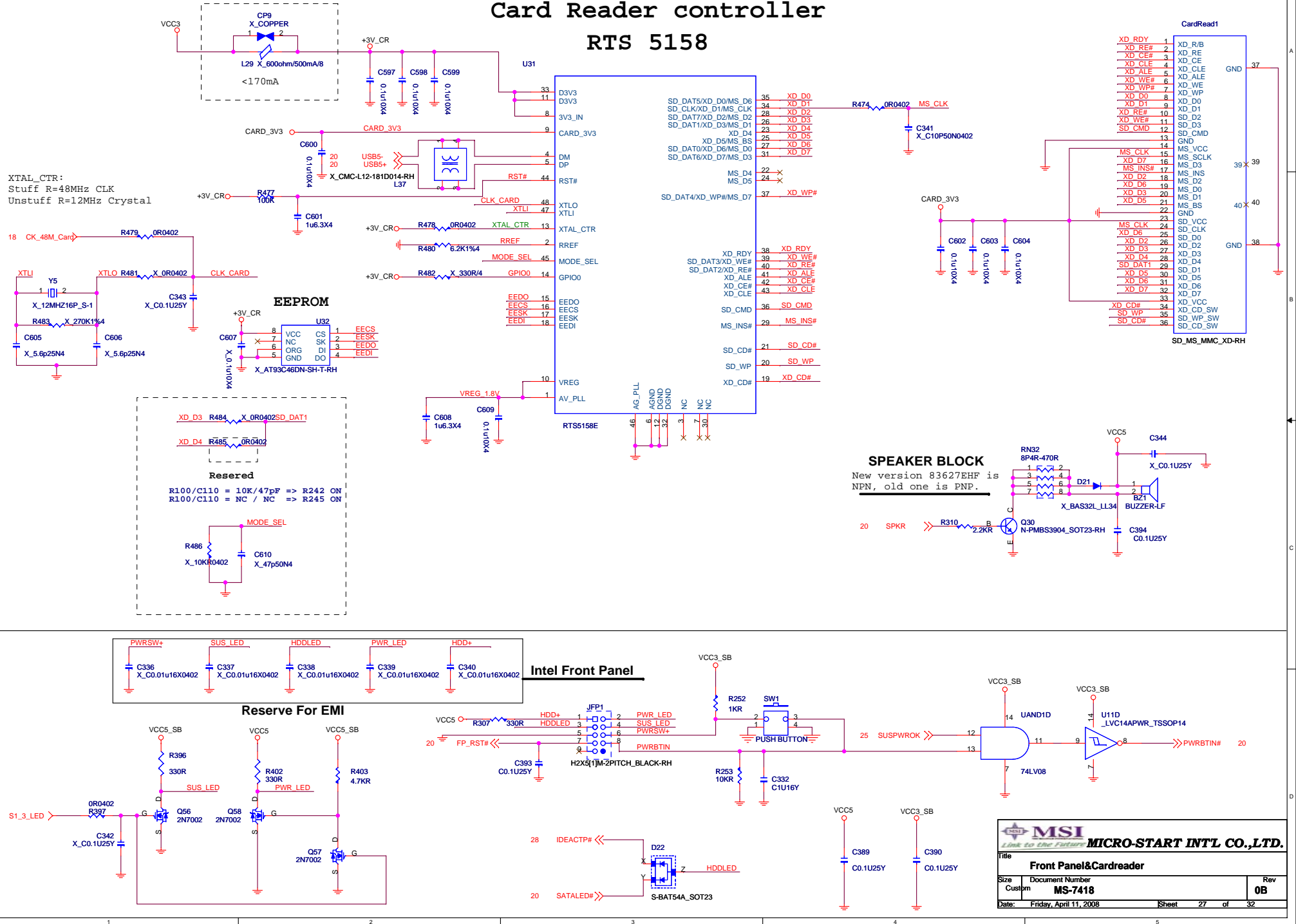




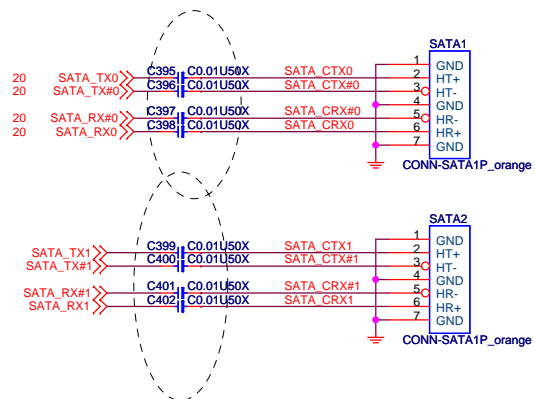


Flash Card Socket

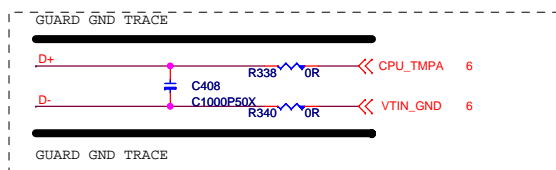
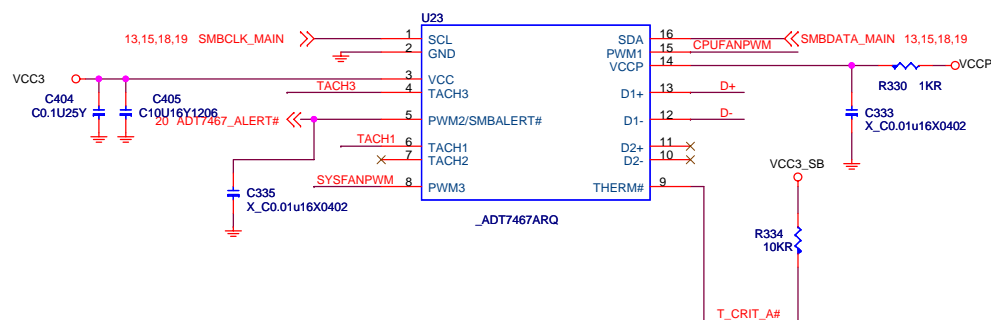
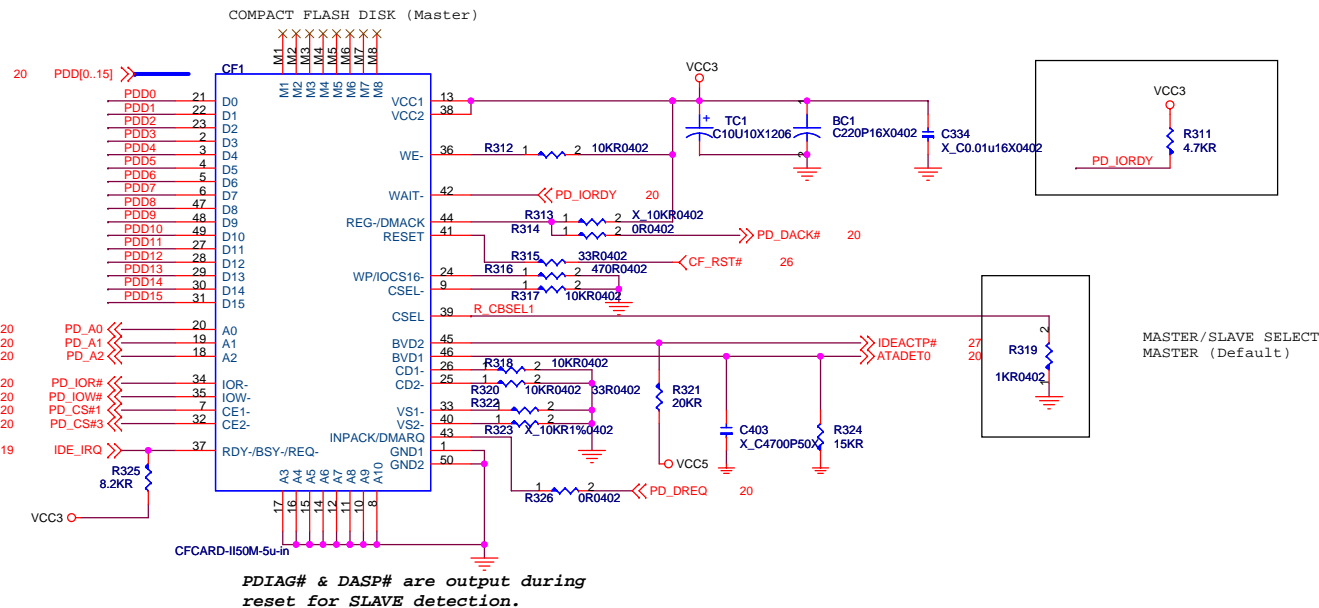
Card Reader controller RTS 5158



SERIAL ATA CONNECTOR BLOCK



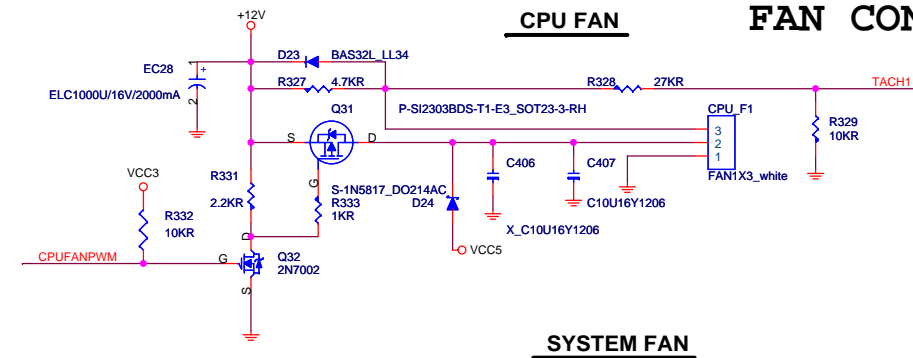
COMPACT FLASH CONNECTOR



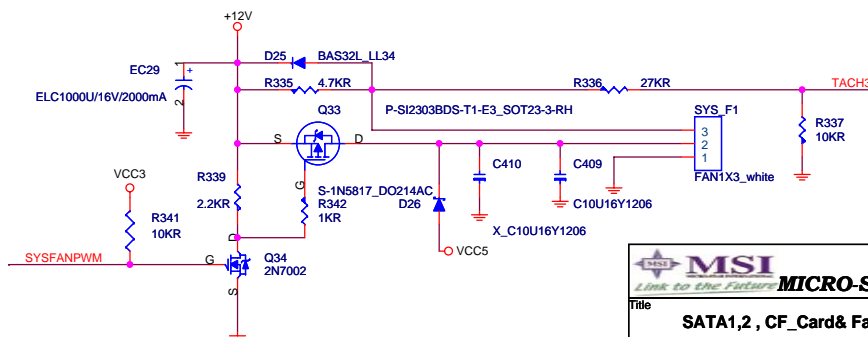
PLACE ADT7467 AS CLOSE AS POSSIBLE TO CPU
GUARD TRACE & D+/D- WIDTH:SPACE= 10:10 MIL(MIN)

CPU FAN

FAN CONTROL



SYSTEM FAN



ACPI Controller

DDR2 1.8V POWER...7.95A

Internal reference $V_{fb}=0.6V$ (+/- 1.5%)
Better than external reference (+/-5%)
==>Using Stand-alone mode

$$V_{fb}=V_{output}*[1.5/(1.5+3.01)]=0.6V \quad V_{output}=1.804V$$

DDR2 1.5V POWER...22.84A

$$V_{fb}=V_{output}*[2/(2+3.01)]=0.6V \quad V_{output}=1.503V$$

VTT1.1V POWER...4.9A

DDR VTT Power

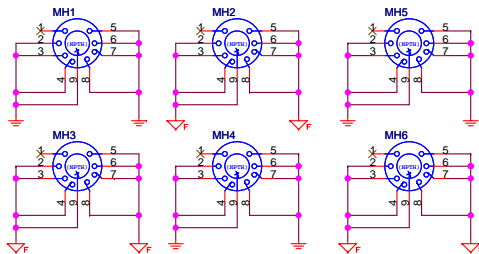


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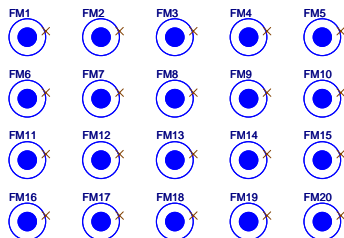
MS7 ACPI CONTROLLER		
Size	Document Number	Rev
	MS-7418	08
Date	Friday, April 11, 2008	Sheet 29 of 32

Auto-BOM Manual Parts

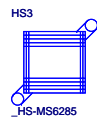
Mounting Holes



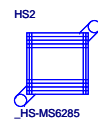
Optics Orientation Holes



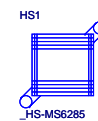
CPU HEAT SINK



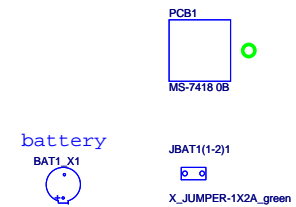
NB HEAT SINK



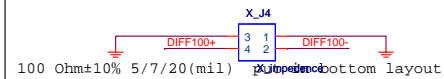
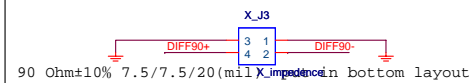
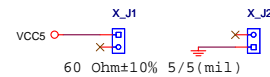
SB HEAT SINK



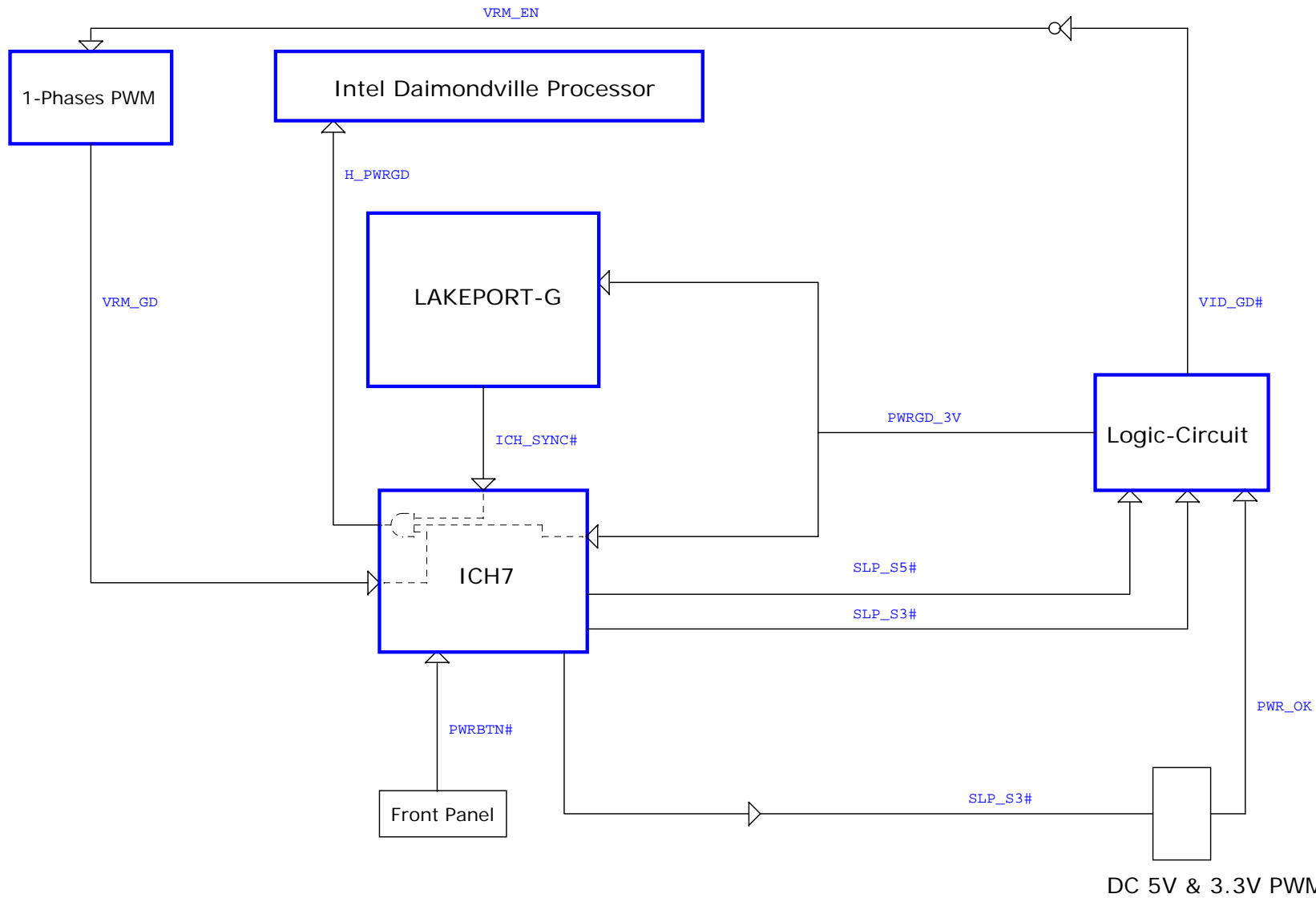
MANUAL PART




Simulation



PWROK MAP



 MICRO-STAR INT'L CO., LTD.			
Title		PWOK MAP	
Size	Document Number	MS-7418	Rev 0B
Date:	Friday, April 11, 2008	Sheet 31 of 32	1

- 0B changed 1-->Pull up follow design guide.(page6)
- 0B changed 2-->Pull up follow design guide.(page6)
- 0B changed 3-->Pull up follow design guide.(page6)
- 0B changed 4-->Pull up follow design guide.(page6)
- 0B changed 5-->Pull up follow design guide.(page6)
- 0B changed 6-->Change R4,R8 to 24.9R, R6,R9 to 49.9R. (page6)
- 0B changed 7-->unstuff R304,stuff R303 follow CRB V0.7.(page7)
- 0B changed 8-->-->change pull up circuit follow CRB V0.7.(page7)
- 0B changed 9-->make sure the power sequence.(page21)
- 0B changed 10-->improve the "PWR_GD" single waveform negative pulse issue. (page8)
- 0B changed 11-->improve the "VRM_GD","ALLPWRGD" single waveform pulse issue. (page29)
- 0B changed 12-->Change resistor value follow design guide.(page19)
- 0B changed 13-->Pull up follow design guide.(page6)
- 0B changed 14-->unstuff R188 follow CRB V0.7.(page19)
- 0B changed 15-->Add SPI Bios interface and strapping resistor. Add PCI interface.
- 0B changed 16-->Add pull down Resistors.(page18)
- 0B changed 17-->Change EC28 same as EC29 for mechanical issue.(page28)
- 0B changed 18-->Change R176 from 5.6k to 1k and change Q8 from 3904 to 2N7002 for UBUF2's pin11 voltage level drop to 2V issue.(page18)
- 0B changed 19-->unstuff R405 for GPIO25.(page20)
- 0B changed 20-->Connect MCHREF voltage to SMVREF0 and SMVREF1.(page10)
- 0B changed 21-->Unstuff PR275,PR276 for no standby power issue.(page25)
- 0B changed 22-->Reserve test point on MCH H_A#32~H_A#35 (page9)
- 0B changed 23-->Remove FWH BIOS interface(page22)
- 0B changed 24-->Change 19V to 12V circuit.(page25)
- 0B changed 25-->Change CPU part number to A09-1320165-I06 (page 6&9)
- 0B changed 26-->Stuff TPM circuit for BIOS bring up(page 22)
- 0B changed 27-->Unstuff MiniPCIE2 circuit(page 15)
- 0B changed 28-->Change CPU,NB,SB heatsink footprint(page 30)
- 0B changed 29-->Change MIC1,HP-OUT Vref circuit(page 24)
- 0B changed 30-->Change VID circuit for jump VID and add 4pcs 10u cap.(page7,8)
- 0B changed 31-->Change choke11 material(page29)
- 0B changed 32-->Add 6 pcs 0.1uF caps for EMI issue(page26)

- 0B changed 33-->
VCCP
 - 1. R40: 14.7k ohm (droop)
 - 2. C24: 0.022uF (RC)
 - 3. R42: 24k ohm (RC)
 - 4. R45: 487 ohm (OCP)
 - 5. R50: 22k ohm (comp)
 - 6. C37: 0.1uF (comp)
 - 7. C22: no pop
- VCC_DDR
 - 1. R350: 3.09k ohm (offset)
 - 2. R354: 1.54k ohm (offset)
- V_1P5_CORE
 - 1. CHOKE11: L04-11A7231-W15

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Title History			
Size	Document Number MS-7418		Rev 0B
Date:	Friday, April 11, 2008	Sheet 32 of 32	